TECHNIQUES FOR TRIPLE AND QUADRUPLE DAMASCENE FABRICATION

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FIELD OF THE INVENTION

The present invention relates to semiconductor device interconnect lines and via plugs which are fabricated using damascene techniques.

BACKGROUND OF THE INVENTION

A semiconductor device such as an IC (integrated circuit) generally has electronic circuit elements such as transistors, diodes and resistors fabricated integrally on a single body of semiconductor material. The various circuit elements are connected through conductive connectors to form a complete circuit which can contain millions of individual circuit elements. Advances in semiconductor materials and processing techniques have resulted in reducing the overall size of the IC circuit elements while increasing their number on a single body. Additional miniaturization is highly desirable for improved IC performance and cost reduction. Interconnects provide the electrical connections between the various electronic elements of an IC and they form the connections between these elements and the device's external contact elements, such as pins, for connecting the IC to other circuits. Typically, interconnect lines form horizontal connections between electronic circuit elements while conductive via plugs form vertical connections between the electronic circuit elements, resulting in layered connections.

A variety of techniques are employed to create interconnect lines and via plugs. One such technique involves a process generally referred to as dual damascene, which includes forming a trench and an underlying via hole. The trench and the via hole are simultaneously filled with a conductor material, for example a metal, thus simultaneously forming an interconnect line and an underlying via plug. Examples of conventional dual damascene fabrication techniques are disclosed in Kaanta et al., "Dual Damascene: A ULSI Wiring Technology", Jun. 11-12, 1991, VMIC Conference, IEEE, pages 144-152 and in U.S. Pat. No. 5,635,423 to Huang et al., 1997.